ABSTRACT OF THE DISCLOSURE

A process for manufacturing a byte selection transistor for a matrix of non volatile memory cells organised in rows and columns integrated on a semiconductor substrate, each memory cell comprising a floating gate transistor and a selection transistor, the process providing the following steps: defining on a same semiconductor substrate respective active areas for the byte selection transistor, for the floating gate transistor and for the selection transistor split by portions of insulating layer; depositing a multilayer structure comprising at least a gate oxide layer, a first polysilicon layer, a dielectric layer on the whole substrate and a second polysilicon layer, characterised in that it comprises the following steps: removing through a traditional photolithographic technique the multilayer structure to form at least a couple of two bands developing substantially in a parallel way to the columns of the matrix of memory cells, the first band being effective to define the gate regions of the byte selection transistor and of the selection transistor, the second band being effective to define the gate region of the floating gate transistor, a portion of the first band further extending on the portion of insulating layer which is adjacent to the byte selection transistor, forming an opening in the portion up to expose the first polysilicon layer, forming a conductive layer in the opening to put said first polysilicon layer in electric contact with said second polysilicon layer.